The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP10 8QQ

INVESTOR IN PEOPLE

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named this certificate and any accompanying documents has re-registered under the Companies Act 80 with the same name as that with which it was registered immediately before re-istration save for the substitution as, or inclusion as, the last part of the name of the words blic limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.

Signed

Dated 21 May 2004

CERTIFIED COPY OF
PRIORITY DOCUMENT

Patents Form 1/77

Patents Act 1977
(Rule 16)

The Patent Office

1/77

THE PATENT OFFICE
25 OCT 2000
LONDON

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office

Cardiff Road
Newport
South Wales
NP9 1RH

1. Your reference — APUK00746

0026105.7

Patent application number *(The Patent Office will fill in this part)* — 25 OCT 2000

2000T00 E570454 1 PA1472
P01/7700 0.00-0026105.7

2. Full name, address and postcode of the or of each applicant *(underline all surnames)* — LSI Logic Europe Ltd

Greenwood House, London Road
Bracknell, Berkshire
RG12 2UB
United Kingdom

Patents ADP number *(if you know it)* -

If the applicant is a corporate body, give the country/state of its incorporation - 8086916607

4. Title of the invention — Header Detect Configuration Within a DVD-Ram Read Device and Methods of Acquiring and Maintaining Phase Lock in a Wobble Phase Lock Loop

5. Name of your agent *(if you have one)* — Hepworth Lawrence Bryer & Bizley

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)* — Merlin House, Falconry Court, Baker's Lane, Epping, Essex CM16 5DQ

Patents ADP number *(if you know it)* — 05608575008

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

Yes

Patents Form 1/77

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	0
Description	20
Claim(s)	6
Abstract	x0
Drawing(s)	6 + 6

10. If you are also filing any of the following, state how many against each item.

Priority documents	–
Translations of priority documents	–
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	–
Request for preliminary examination and search *(Patents Form 9/77)*	–
Request for substantive examination *(Patents Form 10/77)*	–
Any other documents *(please specify)*	Letter

11. I/We request the grant of a patent on the basis of this application.

Signature Hepworth Lawrence Bryer & Bygley Date 25 Oct. 2000

12. Name and daytime telephone number of person to contact in the United Kingdom: Bruce C Dearling 01992 561756

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

Notes

a) If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.

b) Write your answers in capital letters using black ink or you may type them.

c) If there is not enough space for all the relevant details on any part of this form, please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.

d) If you have answered 'Yes' Patents Form 7/77 will need to be filed.

e) Once you have filled in the form you must remember to sign and date it.

f) For details of the fee and ways to pay please contact the Patent Office.

HEADER DETECT CONFIGURATION WITHIN A DVD-RAM READ DEVICE AND METHODS OF ACQUIRING AND MAINTAINING PHASE LOCK IN A WOBBLE PHASE LOCK LOOP

Background to the Invention

This invention relates, in general, to a mechanism and apparatus for acquiring phase lock for data read and write purposes and is particularly, but not exclusively, applicable to phase lock loops (PLLs) in optical data media, such as in the context of digital versatile disc random access memory (DVD-RAM). More especially, the present invention relates to phase acquisition and lock obtained from sinusoidal data tracks of a DVD-RAM read channel that are punctuated into data sectors by header information providing address and location information for the optical disc.

Summary of the Prior Art

With respect to the storage of data on optical storage media, such as on compact disc read only memory (CD-ROM) and DVD-RAM, a selected form of modulation encodes data into the surface of the media. In the context of DVD-ROM or DVD-RAM, an eight-fourteen modulation (efm) scheme is used to encode binary data through the use of data "pits" that are either magnetically or optically inscribed within, or manually embossed/stamped on, the surface of the optical storage medium and undisturbed mirror regions. The length of the pit or complementary mirror is therefore indicative of the encoded binary information, subject to there being no defects associated with the formation of the pit or mirror.

As regards the structure of data segments on an optical storage medium, such data segments (or sectors) spiraling outwardly from a center of the optical storage medium. These data segments are also indexed through the use of a header that is embossed (in this instance physically stamped) onto the surface

of the optical storage medium, with the header providing address and location information, such as track and sector numbers. The headers are individually indexed at the beginning of the disc for use in scanning. The headers have a precisely defined width dimension and are separated by a data sector of defined length. Furthermore, the headers appear in pairs that are physically offset from one another relative to a central datum within each track, with each pair of headers generally followed by an extended mirror region of maximum reflectivity.

From a perspective of data recovery, once on-track, an array of (typically) four photodiodes is used to recover the information stored on the medium, the four photodiodes providing an output voltage that varies according to an amount of reflectivity from the surface of the medium. More particularly, laser light is reflected from the marks and spaces, with a data pit (i.e. a mark) providing an inferior reflectivity and hence a lower voltage than a space (that provides maximum reflectivity and hence maximum voltage).

As regards DVD-RAM, the issue of data encoding is further complicated by the structure employed within the readable/writeable medium. More specifically, in addition to the spiraling and sectorised nature of the modulation data, the marks and spaces are produced within adjacent "lands" and "grooves" that provide a distinct three-dimensional profile to a cross-section of the optical storage medium. The lands and grooves therefore also constitute "tracks" within the storage medium. Moreover, the lands and grooves exhibit a sinusoidal oscillation known as "wobble" which has a frequency of about 157 kiloHertz (at 1x rate) that, as will be understood, is very much lower than the rate of the efm data. The wobble, which is stamped into the optical storage medium, provides speed of rotation information that is critical for operation control of data read and data write functions, with a frequency of the wobble utilized for phase acquisition in a phase lock loop. More specifically, the wobble frequency provides a synchronized write clock having a known linear density of information. Unfortunately, the embossed header regions entirely disrupt (i.e. break) the

continuous sinusoidal oscillation of the wobble. In other words, the wobble simply does not co-exist with header regions. The loss of wobble therefore adversely affects phase acquisition, PLL function and device operation.

In contrast with efm data extraction that takes a sum of the four photodiodes, wobble extraction utilises the so-called "push-pull" signal obtained from the numeric subtraction of adjacent photodiode levels, namely the algebraic expression (A+B)-(C+D) where A, B, C and D are a sequence of adjacent photodiodes in a configuration of a square. For completeness, low pass filtering of the push-pull signal eliminates high frequency noise, such as produced from read frequency (RF) feed-through and any mismatches in, for example, amplification paths, to produce an appropriate signal from which a clock can be derived. As will be understood, in the ideal case, RF errors should be negligible (if not zero), but in practice errors are induced by inaccuracies in the laser and detector alignment with respect to a centre of a particular track on the optical medium. In any event, low frequency noise is nevertheless generally present as a consequence of its introduction by processing and physical properties such as non-planar disc profiles, disc eccentricity, changes in reflectivity and errors in the servo-drive system for control of the laser and detector heads. Existing systems that utilise a low pass filter for wobble recovery are therefore unable to filter out such low pass noise with the consequence that the wobble signal is relatively dirty and interpretational errors may be induced.

As will be understood, when the array of photodiodes encounters each associated pair of headers, the photodiodes produce a maximum or minimum dc deflection (relative to efm data) in the push-pull signal. Moreover, the headers produce an indeterminate number of spikes within the push-pull signal. A transition between each header in the pair also generates a reversal in the dc deflection. In fact, the relative polarity between spikes in the bandpass filtered push-pull signal caused by the headers provides an indication on whether a succeeding data sector appears on a land or a groove, with this polarity

information necessary to instruct the PLL to perform a phase inversion. For completeness, it will be understood that the phase inversion (i.e. a 180° phase shift) always occurs at a transition between data sectors on lands and grooves.

In summary, DVD-RAM read/write operations require a clock to be generated which is phase locked to the wobble signal derived from a readback (or read channel) signal produced by spinning of the optical disc. The wobble is derived from an eccentricity deliberately produced in the track structure of DVD-RAM discs. The eccentric wobble is, however, not continuous and is broken up by embossed header regions (containing track addressing information) and so any phase locked loop (PLL) attempting to lock onto the wobble is generally subject to loss of lock during these header periods.

Summary of the Invention

According to a first aspect of the present invention there is provided a method of synchronising a phase lock loop to an intermittent clock signal applied thereto, the method comprising: seeking to acquire phase lock during periods of the intermittent clock; and holding the phase lock loop in a free-running state during periods when the intermittent clock is absent.

Frequency lock may be acquired in an asynchronous mode.

In one particular embodiment, the intermittent clock signal is derived from a geometric eccentricity associated with a track on an optical disc, and wherein the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity.

The method may further comprise: timing a duration of the intermittent clock signal; and in response to an elapsed duration of the clock signal, placing the phase lock loop in the free-running state in anticipation of an arrival of a header.

It is preferred that the method also include: identifying re-emergence of the clock signal; and seeking to acquire phase lock only after re-emergence of the clock signal has been validated.

The method may include: estimating a signal envelope for the clock signal; bandpass filtering the header region to generate a spike indicative of a header transition; amplifying the signal envelope and the spike to scale the spike relative to the signal envelope, thereby to differentiate in level the signal envelope from the spike; defining a threshold exceeding, in absolute magnitude, the signal envelope; and identifying commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region.

In another embodiment, the method identifies a relative signal level polarity between a first spike and a successive spike to identify a requirement for a phase reversal.

A particular embodiment filters the clock signal in a low pass filter to generate an adaptive slice level signal capable of tracking residual near-dc variations in the clock signal.

Another aspect of the present invention supports the underlying mechanism in a computer program element comprising appropriate computer program code means arranged to make a controller implement procedure to perform the method of the various embodiments previously described above.

In a further aspect of the present invention there is provided a control circuit for coupling, in use, to a phase lock loop arranged to receive an intermittent clocking signal to which the phase lock loop is to be synchronized, the control circuit maintaining, in use, operation control of the phase lock loop, the circuit having: means for determining periods of time when the clocking signal is deemed stable; means for selectively maintaining the phase lock loop in a phase

acquisition state during said periods of time; and means for forcing the phase lock loop to enter a free-running state during periods when the clocking signal is absent or deemed not to be stable.

The intermittent clock signal may be derived from a geometric eccentricity associated with a track on an optical disc and the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity and which each define a data sector, and the circuit may further include: a counter arranged to time the intermittent clocking signal during each data sector; wherein the means for forcing the phase lock loop to enter a free-running state being operationally responsive to time elapsed within each data sector and such that the phase lock loop is placed in the free-running state, based on time elapsed, in advance of an arrival of a header.

A detector may be arranged to identify emergence of a steady state in the clocking signal, the means for forcing the phase lock loop to enter the free-running state being operationally disabled by the detector in response to the steady state.

In a particular embodiment, there is provided: a top hold feedback circuit arranged to estimate a signal envelope for the clock signal; a bandpass filter coupled, in use, to receive the clocking signal, the bandpass filter arranged to filter the header region to generate a spike indicative of a header transition; an amplifier configuration arranged to amplify the signal envelope and the spike thereby to scale the spike relative to the signal envelope to differentiate in level the signal envelope from the spike; data slicing circuitry defining a threshold exceeding, in absolute magnitude, the signal envelope; and a comparator arrangement arranged to identify commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region.

The comparator arrangement preferably comprises first and second comparators respectively configured to process opposite signal senses from the signal envelope, the first and second comparators each providing an output to a controller arranged to identify therefrom the relative signal level polarity between a first spike and a successive spike thereby to identify a requirement for a phase reversal in the phase lock loop.

A low pass filter, responsive to filtering the clocking signal, may be arranged to generate an adaptive slice level signal capable of tracking residual near-dc variations in the clocking signal.

In yet another aspect of the present invention there is provided a DVD-RAM read channel comprising: an array of photodiodes adapted to recover a push-pull signal representation from an optical disc containing data segments interspersed with header regions; and a bandpass filter coupled, in use, to receive the push-pull representation, the bandpass filter operational to filter the header region to generate a spike indicative of a header transition.

The DVD-RAM read channel preferably includes a low pass filter, responsive to a wobble signal emanating from the bandpass filter, the low pass filter arranged to generate an adaptive slice level signal capable of tracking residual near-dc variations in the wobble signal.

In an embodiment, the DVD-RAM read channel further comprises: a top hold feedback circuit arranged to estimate a signal envelope for the clock signal; an amplifier configuration arranged to amplify the signal envelope and the spike thereby to scale the spike relative to the signal envelope to differentiate in level the signal envelope from the spike; data slicing circuitry defining a threshold exceeding, in absolute magnitude, the signal envelope; and a comparator arrangement arranged to identify commencement of a header region by equating

a first spike transition through the threshold as being indicative of the header region.

Advantageously, the present invention provides an improved lock acquisition system for use with DVD-RAM and the like that utilize eccentric track wobble to provide clock and synchronization information. More specifically, the architecture and mechanism employed by the various embodiments of the present invention increases the rate at which lock can be obtained, while the system is considerable more robust in that it is arranged to anticipate loss of the wobble signal to suspend potentially significant and detrimental changes to an acquired phase scenario. In other words, the present invention provides predictive digital control with respect to approaching header regions. Furthermore, the beneficial use of a bandpass filter configured to receive a push-pull signal and therefore takes advantage of the dc offset present in the push-pull signal in the header regions.

The present invention is further capable of handling both land and groove-type headers by virtue of reacting in identical fashion, albeit that trigger points on the recovered wobble signal are in opposite dc senses. Indeed, the present invention is beneficially capable of determining whether or not the header region and following sector is of a land or groove type. Advantageously, the present invention reliably detects header regions and operates to switch-out, freeze-out and generally suspend operation of the wobble PLL, thereby limiting disruption to phase acquisition and phase maintenance during, respectively, asynchronous operation of the wobble PLL (when the PLL is attempting to acquire lock) and synchronous operation when the wobble PLL is attempting to maintain lock.

Brief Description of the Drawings

Exemplary embodiments of the present invention will now be described with reference to the accompanying drawings, in which:

FIG. 1 is a representation of an optical disc;

FIG. 2 illustrates, in some detail, a structure of the optical disc of FIG. 1 and a relationship between tracks on the disc and photodiodes designed to recover reflected laser light;

FIG. 3 illustrates a relationship between a push-pull signal and a recovered clock;

FIG. 4 is a perspective view of tracks exhibiting wobble in a DVD-RAM;

FIG. 5 is a block diagram of wobble signal generation circuitry according to a preferred embodiment of the present invention;

Fig. 6 is a timing diagram illustrating a relationship between a push-pull signal and a wobble signal obtained therefrom;

FIG. 7 is a block diagram of a header slicer circuit according to a preferred embodiment of the present invention, the head slicer circuit for use in FIG. 5;

FIG. 8 is illustrative of a preferred header detection mechanism of the present invention;

FIG. 9 is a header detect logic state machine flow diagram according to a preferred operational mechanism; and

FIG. 10 is a flow diagram of a preferred operating methodology employed by the present invention in acquiring phase lock.

Detailed Description of a Preferred Embodiment

FIG. 1 is a representation of an optical disc 20 showing a spiraling nature (that is greatly exaggerated) of data segments 22-30 outwardly from a centre of the disc 20. Headers 32-40 are diagrammatically represented at the beginning of each data segment 22-30, with each header preceded by a mirror 42-50. FIG. 2 illustrates, in some detail, a structure of the optical disc 20 of FIG. 1 and a relationship between tracks 60-66 ("track 1, 2, 3, 4") on the disc 20 and photodiodes 70-76 designed to recover reflected laser light (not shown). The photodiodes are shown positioned generally centrally with respect to a particular track, namely groove "track 2" (reference numeral 62, 88). More particularly, each track 60-66 is bounded by a wobble eccentricity 78-82 which defines an

area of land 84-86 or groove 88; this is better illustrated in FIG. 4. Modulated data, in the form of pits 90-100 and gaps 102-112, is written substantially at the centre of each track 60-66. As can be seen in FIG. 2, a pair of headers 32, 33 interrupt the continuous flow of the wobble eccentricity 78-82 defining a track 62-66, with the headers 32, 33 followed by a region of mirror 42-52.

FIG. 3 illustrates a relationship between a push-pull signal 130 and a recovered clock 132.

Turning now to FIG. 5, a block diagram of wobble signal generation circuitry 150 according to a preferred embodiment of the present invention. The wobble generation circuitry is shown having an optional mulitplexer 152 that provides the circuitry 150 to acquire an acquired push-pull signal 153-154 from either a suitably configured pre-amplifier or from an integrally formed on-chip function. The multiplexer (MUX) 152 provides a user with an ability to select the source of the error signal, i.e. an external or internal push-pull signal. The push-pull signal 153-154 (illustrated a dual input) is applied to a band pass filter 156, preferably having at least a fifth order characteristic. The bandpass filter is responsive to a rate selector function 158 that selects speed of operation, e.g. 1x, 2x, 4x, 8x of the circuit 150. An output from the bandpass filter 156 is coupled to a positive input of a differential amplifier 160, with an inverting input of the differential amplifier arranged to receive a reference voltage (VREF), which is typically something in the order of 2.5 volts. The differential amplifier 160 provides a substantially sinusoidal wobble signal 164 having a workable peak to trough signal level; hence the differential amplifier typically supports an amplification factor of about 5 or so.

The wobble signal 164 is applied as a first input to a Schmitt trigger 166 that acts to provide a square wave output 169 representative of the wobble signal 164. The extracted wobble signal 164 is further filtered by a very low cut-off low pass filter 170 to generate an adaptive slice level signal 172 which is capable of

tracking any residual near-dc variations in the wobble signal; the adaptive slice level signal 172 is applied as a threshold control input to the Schmitt trigger 166. The low cut-off low pass filter 170 is preferably implemented as a switched capacitor filter. The adaptive slice level signal 172 therefore acts to determine an optimum level about which the wobble is judged; this optimum level generally being symmetrical with respect to a mark-space ratio.

The cut-off low pass filter 170 is provided with a first control input that is a function of a system clock (ASPclk) 176, the control input being managed by an adjustable divider circuit 178 that essentially controls the cut-off of the low pass filter 170 in response to operation of a PLL 179 associated with the wobble. A second control input (labeled "active") 179 acts to activate/deactivate the filter in the identified presence of a header, e.g. the filter is disabled when a header is detected and the second input therefore set, nominally, low to deactivate the cut-off low pass filter 170.

The square wave output 169, in addition to being provided to the PLL 179 associated with the wobble, is also applied to wobble detection logic 180 (the purpose of which will be described subsequently).

In addition to providing a threshold control input to the Schmitt trigger 166, the adaptive slice level signal 172 is also applied to a header slicer circuit 182 that also receives the wobble signal 164 as an input. The header slicer circuit 182 provides control outputs (or header region detection signals) hdpos 184 and hdneg 186 that are pulsed with each large signal excursion beyond a magnitude of a wobble envelope; this will be described in more detail in relation to FIGs. 7 and 8. The header slicer circuit 182 is responsive to two further control inputs (shown as parallel buses providing control data words to the header slicer circuit 182), namely wobble top hold discharge ratio control 188 and header slicer control level 190; again the purpose of these will be described subsequently.

The hdpos 184 and hdneg 186 pulses are provided to a header read controller 190 that is further responsive to the wobble detector 180. The header read controller 190, besides providing a control output 192 for ancillary circuitry, also provides a further output 194 (hd_sync) to a counter 196. The wobble PLL 179 is operationally responsive to the header read controller, albeit that the wobble PLL is effectively controlled, in a preferred embodiment, by an output PLL_enable emanating from the counter 196.

The bandpass filter 156 replaces the low pass in conventional DVD-RAM circuits. The bandpass filter 156 operates to reject both high frequency and low frequency noise from the incoming push-pull signal 153, 154 but is pitched to allow the wobble signal 164 (which is embedded in the push-pull signal) to pass through. Furthermore, use of the bandpass filter 156 (as opposed to a low pass filter) causes a spike at each transition of the header dc level. The affect of bandpass filtering the push-pull signal 153, 154 in the generation of the wobble signal is shown in FIG. 6.

It will be appreciated that offsets in the bandpass filter 158 and amplifier 160 configuration will generally cause the resultant wobble signal 164 not to be centred on VREF 162. Consequently, the low pass filter 170 is used to generate the slice level to take account of dc errors. Consequently, the circuitry could be simplified with removal of the low pass filter chain, but this would be detrimental to operational performance since such removal would assume centralized location of the wobble signal. The bandpass filtering scheme employed in a preferred embodiment therefore avoids error frequency components.

Read frequency data associated with the header is destroyed by the process of bandpass filtering.

The wobble detection logic 180 is used to identify periods when the system is actually in data segments, as opposed to header and mirror regions. The wobble

detection logic 180 is configured to measure the periods between transitions by over-sampling with a high-speed clock such that identification of, say, four regular periods within a given tolerance is adjudged to be representative of a valid period of wobble in a data sector.

Briefly referring to FIG. 6, it can be seen that these is a general correspondence between the push-pull signal 153, 154 and the derived wobble signal 164. However, looking specifically to the header regions, it should be noted that large dc offsets 200-206 (i.e. signal excursion spikes) occur at the transition into, out of and between headers 32, 33. Intermediate to these spikes 200-206 are regions of spurious noise that must be disregarded. It has been recognized in the present invention that only the initial spike 200 is certain to identify a header region and that the reminder of the header contains an indeterminate number of spikes and with differing dc offsets.

FIG. 7 is a block diagram of a header slicer circuit 182 according to a preferred embodiment of the present invention. The header slicer circuit 182 takes judicious advantage of the fact that a DC offset exists in the signal during the header regions. As regards a general architecture, the wobble signal provides both a positive input to a top hold comparator 250 and first inputs to header positive level (hdpos) and header negative level (hdneg) comparators 252 and 254, respectively. A top hold digital to analog converter (DAC) 256 receives a reference voltage (VREFH) 258 that, in a preferred embodiment of the present invention, is selected to be equal to about VREF+VREF/2.5. An output (Vtop) 257 from the top hold DAC 256 provides first inputs to parallel top threshold amplifiers 260-262 that provide signal amplification, respectively, for positive and negative spikes (as determined relative to a, preferably, central position within an envelope of the wobble signal). The top hold DAC 256 also receives the wobble slice level 172 as an input, and the top threshold amplifiers 260-262 further also receive the wobble slice level 172 as respective second inputs. An output from the top threshold comparator 250 is looped back through top hold

logic 264 to provide a control data word 266 to the top hold DAC 256. The top hold logic 264 is responsive to the system clock (ASPclk) 176 and the wobble top hold discharge ratio control word. The top hold logic 264 therefore acts to find Vtop and operates to accelerate the top hold DAC 256 to this level. The top threshold amplifiers 260-262 are selected to amplify respective input signals by a factor of, say, 2.5, but it should be noted that the amount of amplification is arbitrary and merely sufficient to cover an anticipated range spike 200-206 voltage levels. Conceivably, the top threshold amplifier could be realized as a single amplifier having a switchable input source, but a complementary pair of amplifiers is conceptually more easily understood.

As will be appreciated, the feedback loop produced by the combination of the top hold DAC 256, the output of the top threshold comparator 250 and the top hold logic 264 operate to perform a convergence such that an output voltage Vtop is equal to the peak output of the wobble envelope. The wobble top discharge ratio, as will be understood, provides an auto discharge capability that tracks degradation in the wobble signal level. In other words, the wobble top discharge ratio controls a rate by which the peak voltage will decay during any absence of an input signal, with this taking into account the fact that Vtop 257 will always decay. The header slicer circuit 182 is therefore self-adjusting in nature to take into account generally slow variations in the envelope amplitude of the wobble signal 164.

Respective outputs of the top threshold amplifiers 260, 262 provide first control signals 270, 272 (vpos_slice_dac and vneg_slice_dac) to first and second header slice DACs 274, 276 respectively. The first and second headers slice DACs 270, 272 also receive (as control inputs) the header slicer level 190 and the wobble slice level 172. An output (vhd_pos) 280 from the first header slicer DAC provides a second input to the header positive level (hdpos) comparator 252, whereas an output (vhd_neg) 282 from the second header slicer DAC 276 provides a second input to the header negative level (hdneg) comparator 254.

The configuration of the header slicer 182 therefore ensures that each spike in each header generates an output pulse (hdpos or hdneg) at the outputs of the respective header positive level (hdpos) comparator 252 or the header negative level (hdneg) comparator 254.

The header slicer level 190 is a control parameter that sets the threshold at which the header slicer comparator triggers.

In operation, the feedback loop comprising the top threshold comparator 250, top hold logic 264 and top hold DAC generates a voltage, Vtop 257, which will converge to a value equal to the peak amplitude of the wobble signal 164. The Vtop signal 257 will be amplified both in a positive sense to generate another voltage, vpos_slice_dac, and in a negative sense to generate vneg_slice_dac. The vpos_slice_dac and vneg_slice_dac voltages will therefore be equal in magnitude but opposite in sign and symmetrical around the wobble slice level voltage 172. The two header slice DACs 274-276 (Header Slicer DAC1 and Header Slicer DAC2) are used to generate a further pair of voltages, vhd_pos and vhd_neg which are bounded by: i) vpos_slice_dac; ii) wobble slice level + Vtop; iii) vneg_slice_dac; and iv) wobble slice level - Vtop. The exact level of vhd_pos and vhd_neg, within these bounds, is determined by a user controlled parameter, Header Slicer Level 190. The levels of vhd_pos and vhd_neg are selected such that they sit at a level which is crossed by the peaks in the bandpass filtered wobble signal (resulting form a high rate of change in the dc level that exist in the push-pull signal at the header region boundaries), but not crossed by the wobble signal elsewhere.

Turning now to FIG. 8, the details of the signal relationships within the header detection circuitry are shown; these signals having been produced by in the header slicer circuit 182. As can be seen from this figure, the start of each header region 32, 33 can be determined by a pulse 300-306 on either hdpos or hdneg outputs. By way of providing a preferred, but exemplary, scaling for the

various voltages, the preferred embodiment assumes a full-scale deflection of, say, ±1.8V from the wobble slice level 168. The ±1.8V level equates to the outer vpos_slice_dac and the vneg_slice_dac limits. With Vtop 257 having a peak of ±0.75V above the wobble slice level 168, with the difference between vpos_slice_dac and Vtop 257 represents the operational range of the first header slicer DAC 274, whereas the operational range of the second header slicer DAC 276 between vneg_slice_dac and –Vtop. To avoid false triggering of header detection, vhd_pos and vhd_neg are set marginally above the ±0.75V envelope of the wobble signal 168. As can be seen, any transient spike 310-316 (associated with passage into, between, across or out of a header) at least peaks at but preferably clips the thresholds of vpos_slice_dac and vneg_slice_dac, with the transient spike 31-316 causing simultaneous generation of pulses 300-306 on either hdpos or hdneg outputs.

It should be noted that the sequence of the pulses 300-306 on hdpos and hdneg, as shown in FIG. 8, are indicative of a transition from a grooved data sector to a land data sector.

The sliced wobble signal 168 and the hdpos and hdneg pulses are passed to a header detector state machine, such as realised by software or a dedicated processor. The state machine is, in fact, represented in FIG. 5 as a combination of elements including the wobble detection logic 180 and the header read controller 190. The purpose of the state machine, amongst other things, is to generate a trigger pulse at the beginning of every header region, the header region being defined as the first header in any complementary pair of headers (e.g. headers 32 and 33 of FIG. 2).

A state transition diagram for the state machine flow is shown in FIG. 9. The state machine is enabled when the READ input is high, indicating that the device (e.g. a machine supporting a DVD-multi architecture) is in a read mode 350. After the assertion of READ, the state machine will enter the initial state 352,

where it will remain 354 until it detects the presence 356 of a valid wobble sequence. The presence 356 of a valid wobble sequence is detected by monitoring the period between positive edge transitions of the sliced wobble stream (168 of FIG. 5) by counting time intervals using a much faster clock; no phase locked relationship between the clock and sliced wobble stream 168 is assumed. In a preferred embodiment, when 4 or more consecutive period counts agree within a predetermined tolerance, then a valid incoming wobble stream is assumed to be present. This test is done so as to allow time for the front-end analogue circuitry to arrive at the correct convergence points for the slice thresholds after the assertion of READ.

Once a valid wobble stream has been determined to be present, then the state machine arms itself to "look for a header"; this is the armed state 358. The state machine will remain 360 in the armed state 358 until an input pulse is received either on the hdpos or hdneg inputs from the analogue header slicer circuit 182.

Once a pulse 300-306 is received 362 on either the hdpos or hdneg input, then the state machine enters the header state 364. In this header state 364, all subsequent pulses on the hdpos and hdneg inputs are ignored until the state machine transitions back 366 into the armed state. (The skilled addressee will recall that subsequent pulses are ignored because the bandpass wobble signal will become indeterminate during the header region). The state machine will remain in the header state 364 until a valid wobble sequence is detected once again, at which point it will revert to the armed state 358.

When in the armed state, the state machine also notes which of either a hdpos or hdneg input activates first on the onset of a header region, with this information used to identify whether a succeeding data sector is land or groove.

The process of the state machine can also be understood with regard to the flow diagram of FIG. 10. Initially, at disc spin-up 400, the system (such as a DVD-

RAM, DVD-multi or the like) operates in an asynchronous mode 402 before phase lock is acquired. During spin-up, the header index at the beginning of the disc is read to obtain/display address information or an index. The device/system of the present invention is therefore free-running at an arbitrarily selected frequency. At some point, the wobble signal is identified 406 by the wobble detector 180 and frequency and phase acquisition in the wobble PLL 179 is allowed to commence.

However, upon detection 410-412 of a header region, the phase acquisition is suspended 414 and the wobble PLL 179 is prevented from moving off-phase or off-frequency, i.e. the output of the wobble PLL is held. At re-detection 416-418 of the wobble signal 164, the wobble PLL 179 returns to phase acquisition/maintenance and the process continues in this on-off operational mode determined by the presence or absence of a valid wobble signal. In other words, detection of an onset of each header regions place the wobble PLL 179 in a free-run mode until the header region has passed, thereby mitigating the likelihood that the wobble PLL will loose lock during the header regions.

With the re-detection of valid wobble, the wobble detector 180 also provides 420 a control signal to the header read controller 190 that can then instigate and synchronise circuit operation, in general. For example, the header read controller 190 generates a counter reset 422 and control signal (hd_sync) 194 that causes the counter 196 both to reset and to start over-sampling wobble periods to increment 424 its internal count. So long as the counter is operational, then the wobble PLL 179 is operational.

In a particular aspect and embodiment of the present invention, the hd_sync header synchronisation pulse is used as a trigger for PLL operation. It will be appreciated that the hd_sync header synchronisation pulse is triggered at a time delayed from the first pulse on either the hdpos or hdneg outputs, the time delay being the difference between the first pulse and confirmation that a valid wobble

has been re-established. Many aspects of DVD-RAM read circuitry (e.g. VGA gain, dc restoration values, PLL) need to be switched during the header boundaries. The switching of such circuitry is controlled by header read controller 190. As previously indicated, headers are accurately stamped across the optical medium and so by using a system employing the counter 196 clocked by both the sliced wobble sequence and the oscillator clock (which runs at 186x the rate of the wobble stream) to predict 426 the onset of the next header region, the system of the present invention can predict the next header and disable the wobble PLL slightly in advance of header region boundaries. More specifically, when the count associated with over-sampling the sliced wobble approaches/nears 426 a value indicative of an imminent header then the wobble PLL 179 can be placed in the free-running, i.e. suspended phase acquisition, mode.

This predictive aspect of the system circumnavigates problems that otherwise exist in schemes where a change in the signal due to the onset of a header has to be detected before control signals for that header region can be issued. The control of the counter settings are also made available to the user so that user control can be exercised on the switching of these control signals. The counters are reset with every hd_sync header synchronisation pulse. The counter 196 therefore effectively controls operation of the wobble PLL 179 for the majority of time.

In summary, therefore, the present invention identifies a wobble window in which the PLL can only acquire phase acquisition. An aspect of the invention utilises a counter to predict successive header regions to improve synchronisation and avoid minor disruptions to the PLL induced by over-running a subsequent header. The use of the counter is, however, preferred and the system could nevertheless operate (in a sub-optimum way) by reacting to header detection to suspend wobble PLL operation.

Alternative embodiments of the invention may be implemented as computer program code encoded on a computer program product for use with a computer system. It is expected that such a computer program product may be distributed as a removable medium with accompanying printed or electronic documentation (e.g. shrink-wrapped software), preloaded with a computer system or distributed from a server or electronic bulletin board over a network (e.g. the Internet or World Wide Web). A series of computer instructions can therefore either be fixed on a tangible medium or fixed in a computer data signal embodied in a carrier wave that is transmittable to a computer system using wireline or wireless transmission techniques. The removable (i.e. tangible) medium may be a computer readable media, such as a diskette, CD-ROM, DVD-ROM or RAM, fixed disc, magneto-optical discs, ROMs, flash memory or magnetic or optical cards. The series of computer instructions embodies all or part of the functionality previously described herein with respect to the system.

Software embodiments of the invention may be implemented in any conventional computer programming language. For example, preferred embodiments may be implemented in a procedural programming language (e.g. "C") or an object oriented programming language (e.g. "C++").

Although the preferred operating method is realised by general or specific-purpose processor or logic circuits programmed with suitable machine-executable instructions, hardware components may possibly be used to implement certain features of the present invention. Of course, the present invention may be performed by a combination of hardware and software.

It will, of course, be appreciated that the above description has been given by way of example only and that modifications in detail may be made within the scope of the present invention.

We claim:

Claims

1. A method of synchronising a phase lock loop to an intermittent clock signal applied thereto, the method comprising:

seeking to acquire phase lock during periods of the intermittent clock; and

holding the phase lock loop in a free-running state during periods when the intermittent clock is absent.

2. The method according to claim 1, further comprising acquiring frequency lock in an asynchronous mode.

3. The method according to claim 1 or 2, wherein the intermittent clock signal is derived from a geometric eccentricity associated with a track on an optical disc, and wherein the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity.

4. The method according to claim 3, further comprising:

timing a duration of the intermittent clock signal; and

in response to an elapsed duration of the clock signal, placing the phase lock loop in the free-running state in anticipation of an arrival of a header.

5. The method according to claim 4, further comprising:

identifying re-emergence of the clock signal; and

seeking to acquire phase lock only after re-emergence of the clock signal has been validated.

6. The method according to claim 3, 4 or 5, further comprising:

estimating a signal envelope for the clock signal;

bandpass filtering the header region to generate a spike indicative of a header transition;

amplifying the signal envelope and the spike to scale the spike relative to the signal envelope, thereby to differentiate in level the signal envelope from the spike;

defining a threshold exceeding, in absolute magnitude, the signal envelope; and

identifying commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region.

7. The method according to claim 6, further comprising:

identifying a relative signal level polarity between a first spike and a successive spike to identify a requirement for a phase reversal.

8. The method according to claim 6 or 7, further comprising:

filtering the clock signal in a low pass filter to generate an adaptive slice level signal capable of tracking residual near-dc variations in the clock signal.

9. A computer program element comprising computer program code means arranged to make a controller implement procedure to perform the method of any of claims 1 to 8.

10. The computer program element of claim 9, embodied on a computer readable medium.

11. A control circuit for coupling, in use, to a phase lock loop arranged to receive an intermittent clocking signal to which the phase lock loop is to be synchronized, the control circuit maintaining, in use, operation control of the phase lock loop, the circuit having:

means for determining periods of time when the clocking signal is deemed stable;

means for selectively maintaining the phase lock loop in a phase acquisition state during said periods of time; and

means for forcing the phase lock loop to enter a free-running state during periods when the clocking signal is absent or deemed not to be stable.

12. The control circuit of claim 11, wherein the intermittent clock signal is derived from a geometric eccentricity associated with a track on an optical disc and the geometric eccentricity is interspersed by regularly spaced header regions that disrupt the geometric eccentricity and which each define a data sector, the circuit further including:

a counter arranged to time the intermittent clocking signal during each data sector; wherein

the means for forcing the phase lock loop to enter a free-running state being operationally responsive to time elapsed within each data sector and such that the phase lock loop is placed in the free-running state, based on time elapsed, in advance of an arrival of a header.

13. The control circuit of claim 12, further comprising:

a detector arranged to identify emergence of a steady state in the clocking signal, the means for forcing the phase lock loop to enter the free-running state being operationally disabled by the detector in response to the steady state.

14. The control circuit of claim 12 or 13, further comprising:

a top hold feedback circuit arranged to estimate a signal envelope for the clock signal;

a bandpass filter coupled, in use, to receive the clocking signal, the bandpass filter arranged to filter the header region to generate a spike indicative of a header transition;

an amplifier configuration arranged to amplify the signal envelope and the spike thereby to scale the spike relative to the signal envelope to differentiate in level the signal envelope from the spike;

data slicing circuitry defining a threshold exceeding, in absolute magnitude, the signal envelope; and

a comparator arrangement arranged to identify commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region.

15. The control circuit of claim 14, wherein the comparator arrangement comprises first and second comparators respectively configured to process opposite signal senses from the signal envelope, the first and second comparators each providing an output to a controller arranged to identify therefrom the relative signal level polarity between a first spike and a successive spike thereby to identify a requirement for a phase reversal in the phase lock loop.

16. The control circuit of claim 13, 14 or 15, further comprising:

a low pass filter, responsive to filtering the clocking signal, arranged to generate an adaptive slice level signal capable of tracking residual near-dc variations in the clocking signal.

17. A DVD-RAM device comprising the control circuit of any of claims 11 to 16.

18. A DVD-RAM read channel comprising:

an array of photodiodes adapted to recover a push-pull signal representation from an optical disc containing data segments interspersed with header regions; and

a bandpass filter coupled, in use, to receive the push-pull representation, the bandpass filter operational to filter the header region to generate a spike indicative of a header transition.

19. The DVD-RAM read channel of claim 18, further comprising:

a low pass filter, responsive to a wobble signal emanating from the bandpass filter, the low pass filter arranged to generate an adaptive slice level signal capable of tracking residual near-dc variations in the wobble signal.

20. The DVD-RAM read channel of claim 18 or 19, further comprising:

a top hold feedback circuit arranged to estimate a signal envelope for the clock signal;

an amplifier configuration arranged to amplify the signal envelope and the spike thereby to scale the spike relative to the signal envelope to differentiate in level the signal envelope from the spike;

data slicing circuitry defining a threshold exceeding, in absolute magnitude, the signal envelope; and

a comparator arrangement arranged to identify commencement of a header region by equating a first spike transition through the threshold as being indicative of the header region.

21. The DVD-RAM read channel of 20, wherein the comparator arrangement comprises first and second comparators respectively configured to process opposite signal senses from the signal envelope, the first and second comparators each providing an output to a controller arranged to identify therefrom the relative signal level polarity between a first spike and a successive spike thereby to identify a requirement for a phase reversal in a phase lock loop within the DVD-RAM read channel.

21. A DVD player or recorder substantially as hereinbefore described with reference to FIGs. 5 and 8 to 10 of the accompanying drawings.

22. A method of synchronising a phase lock loop to an intermittent clock signal applied thereto, substantially as hereinbefore described with reference to FIG. 10 of the accompanying drawings.

21. A control circuit for a phase lock loop, substantially as hereinbefore described with reference to FIGs. 5 and 8 to 10 of the accompanying drawings.

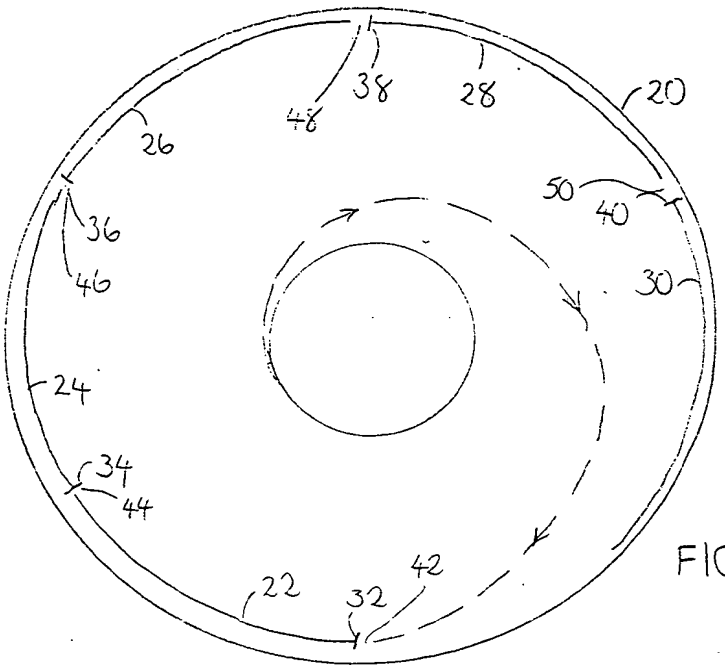


FIG. 1: Prior Art

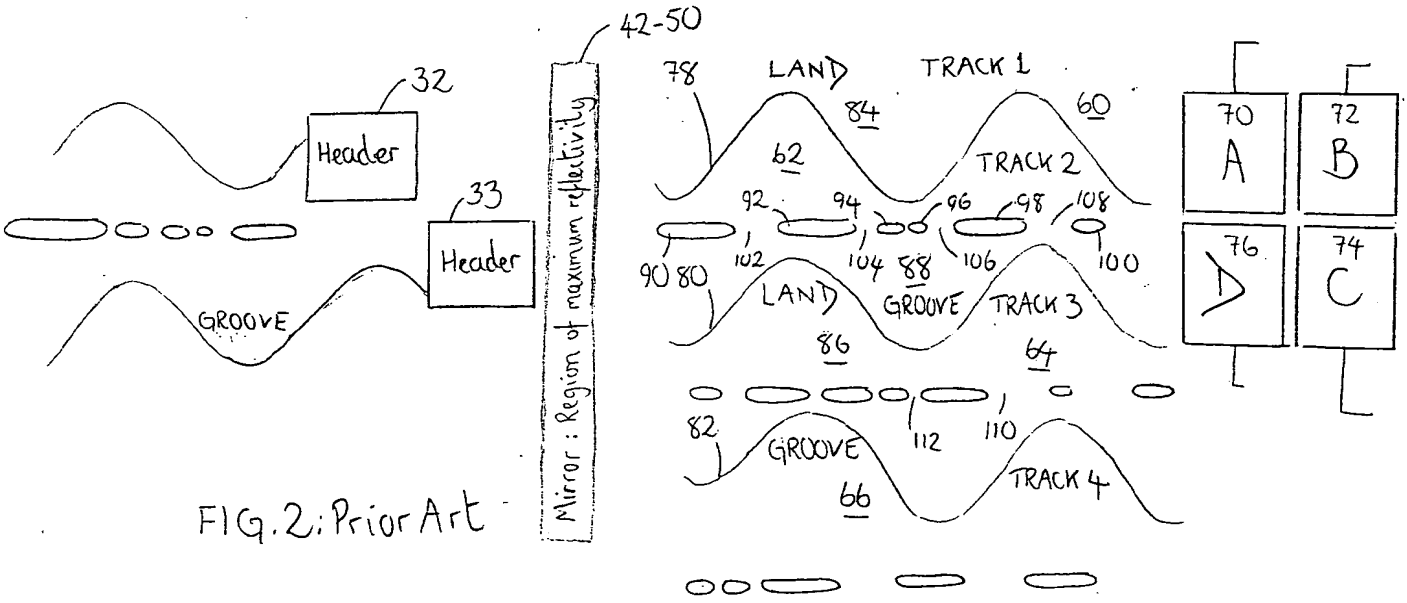


FIG. 2: Prior Art

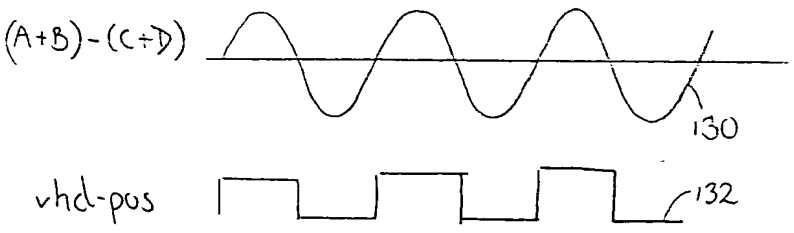


FIG. 3: Prior Art

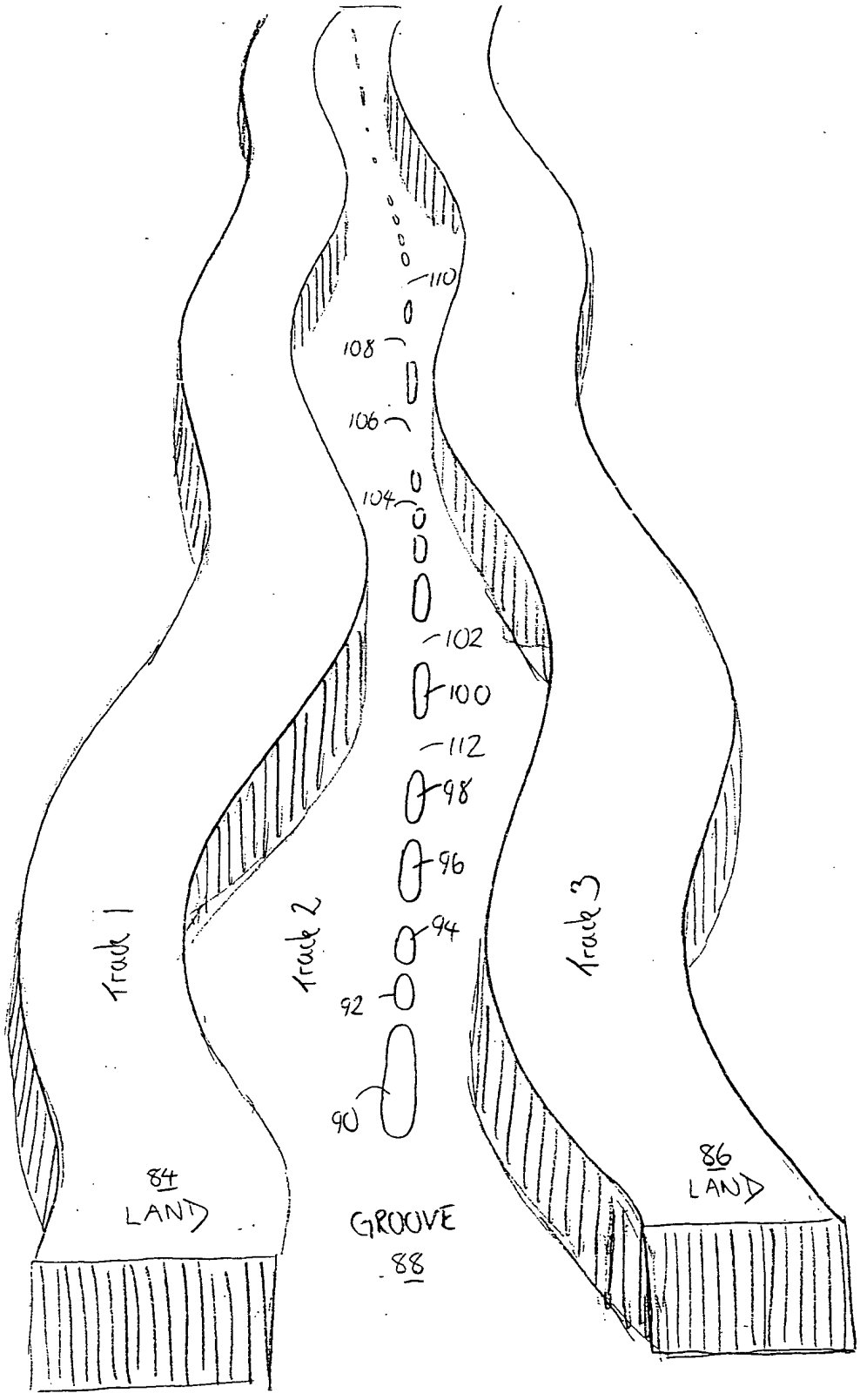


FIG. 4: Prior Art

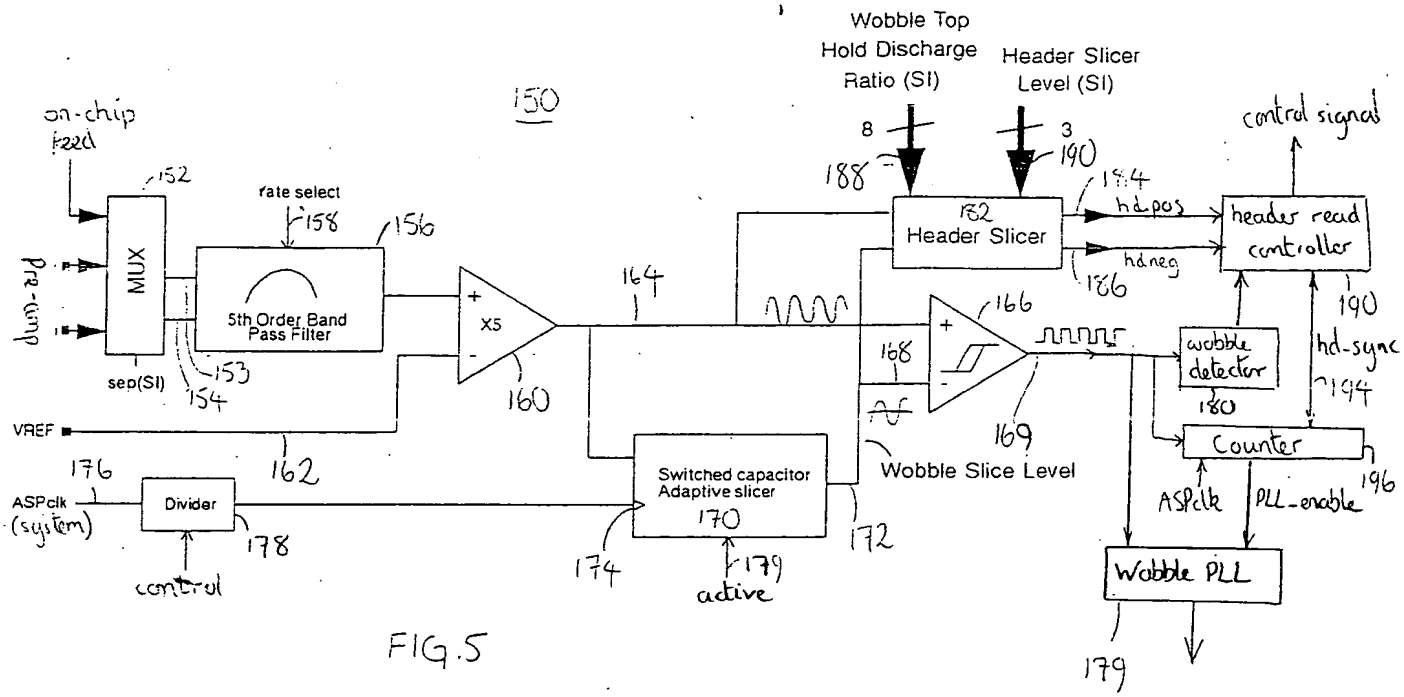

150
on-chip feed
152
MUX
dum-sel
sep(SI)
153
154
rate select
158
156
5th Order Band Pass Filter
X5
160
164
VREF
162
176
ASPclk (system)
Divider
178
control
Switched capacitor Adaptive slicer
170
174
179
active
Wobble Top Hold Discharge Ratio (SI)
8
188
Header Slicer Level (SI)
3
190
182
Header Slicer
184
hd_pos
hd_neg
186
control signal
header read controller
190
hd-sync
194
166
168
169
Wobble Slice Level
172
wobble detector
180
Counter
196
ASPclk
PLL_enable
Wobble PLL
179

FIG.5

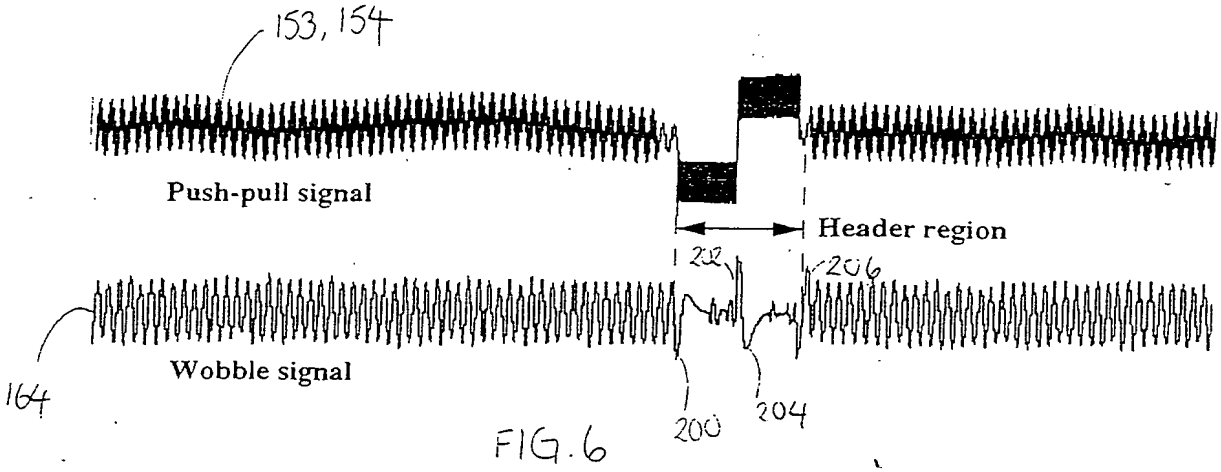

153, 154
Push-pull signal
Header region
202
206
Wobble signal
164
200
204

FIG.6

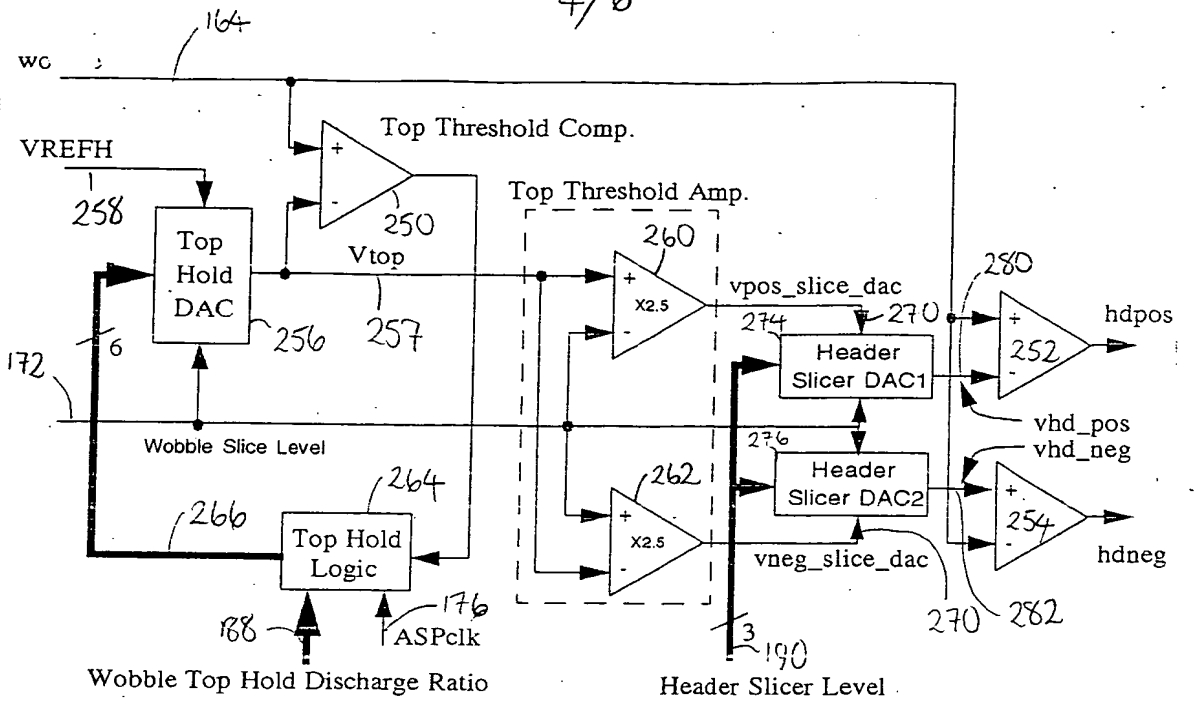

164
WC
Top Threshold Comp.
VREFH
258
250
Top Threshold Amp.
Top Hold DAC
256
Vtop
257
260
vpos_slice_dac
280
270
274
hdpos
Header Slicer DAC1
252
172
6
Wobble Slice Level
vhd_pos
vhd_neg
276
Header Slicer DAC2
262
264
266
Top Hold Logic
254
hdneg
vneg_slice_dac
270
282
188
176
ASPclk
3
190
Wobble Top Hold Discharge Ratio
Header Slicer Level

FIG.7

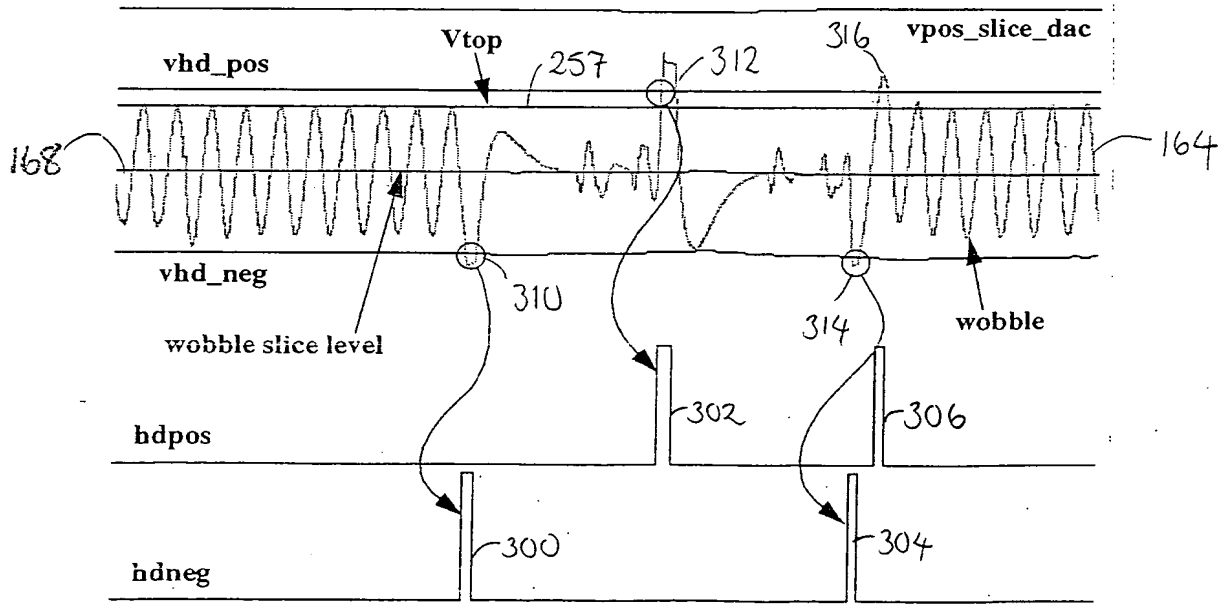

vhd_pos
Vtop
257
312
316
vpos_slice_dac
168
164
vhd_neg
310
314
wobble slice level
wobble
hdpos
302
306
hdneg
300
304

FIG.8

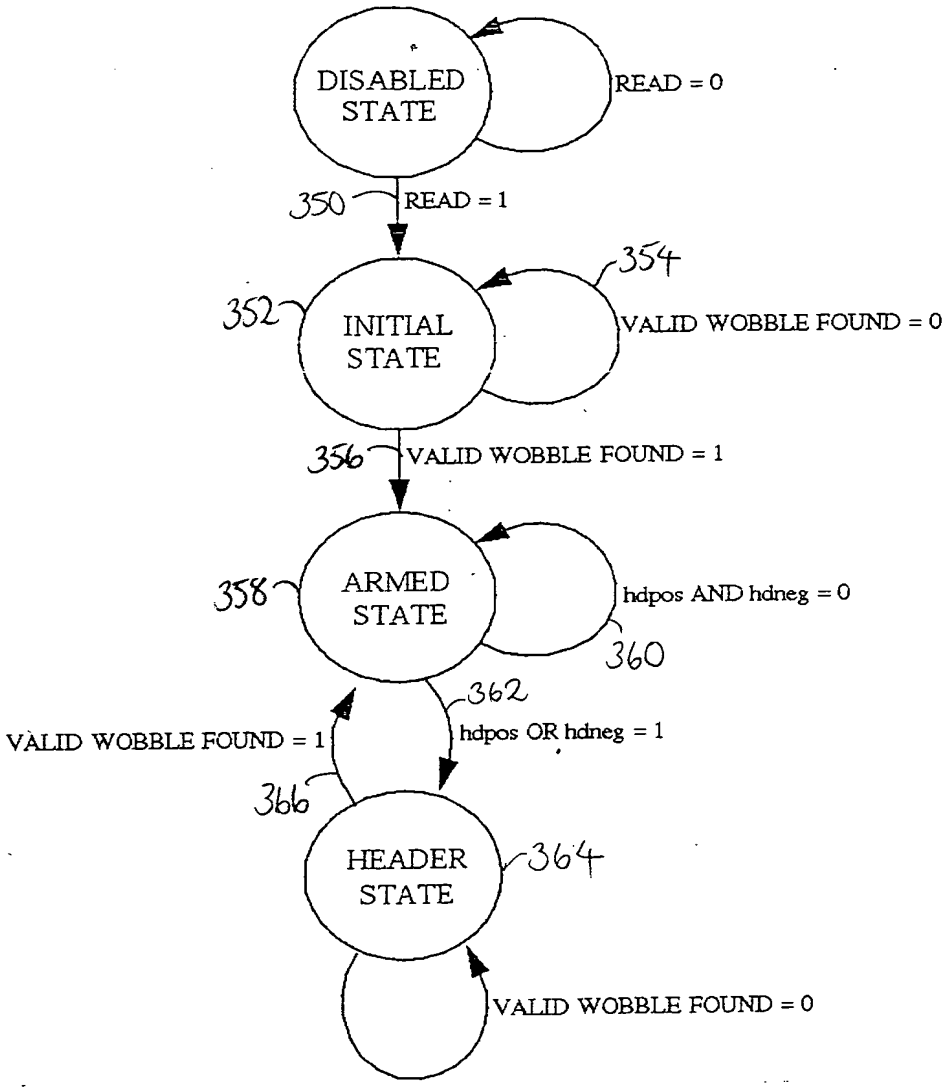
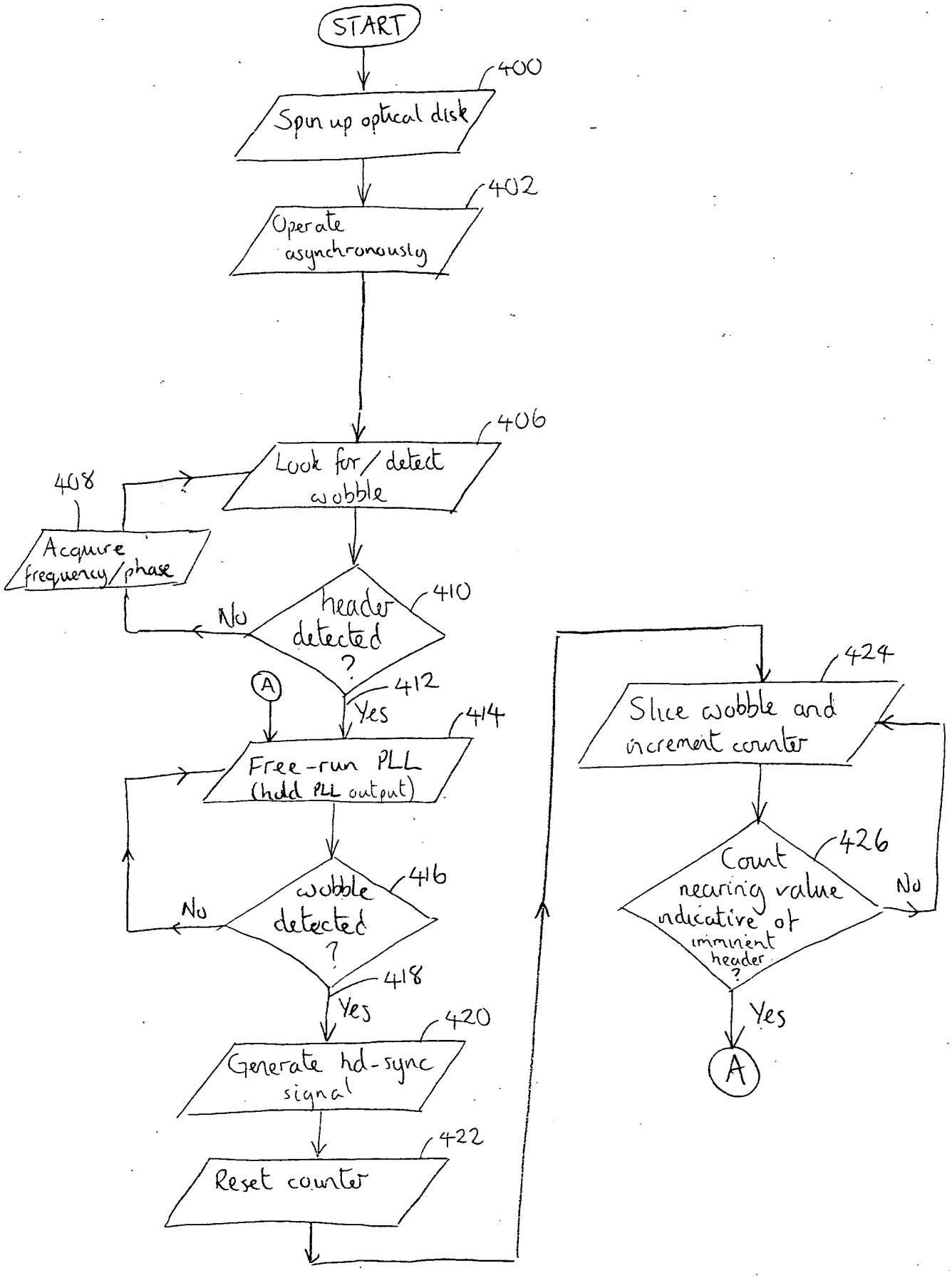

DISABLED STATE
READ = 0
350
READ = 1
354
352
INITIAL STATE
VALID WOBBLE FOUND = 0
356
VALID WOBBLE FOUND = 1
358
ARMED STATE
hdpos AND hdneg = 0
360
362
hdpos OR hdneg = 1
VALID WOBBLE FOUND = 1
366
HEADER STATE
364
VALID WOBBLE FOUND = 0

FIG. 9


START
400
Spin up optical disk
402
Operate asynchronously
406
Look for / detect wobble
408
Acquire frequency/phase
410
header detected ?
No
412
Yes
A
414
Free-run PLL (hold PLL output)
416
wobble detected ?
No
418
Yes
420
Generate hd-sync signal
422
Reset counter
424
Slice wobble and increment counter
426
Count nearing value indicative of imminent header ?
No
Yes
A

THIS PAGE BLANK (USPTO)